

Attorney
Dkt. No.

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Client Ref.

284032

01F171

**INFORMATION DISCLOSURE STATEMENT
BY APPLICANT**



Applicant: YAMADA et al

Appln. No.: 09/993,967

Filing Date: November 27, 2001

Date: February 11, 2002

Page 1 of 1

Examiner:

Group Art Unit: 2812

U.S. PATENT DOCUMENTS

Examiner's Initials*	Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
	AR					
	BR					
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FOREIGN PATENT DOCUMENTS

						Abstract		Readily Available		
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OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

YR	T. Hamamoto et al., "well concentration: A Novel Scaling Limitation Factor derived from DRAM, Retention Time and Its Modeling" IEDM Tec. Dig., P915-918			
ZR				
AAR				
BBR				

Examiner

Date Considered: 11/29/04

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

FORM PTO-1449 (modified)
 To: U.S. Department of Commerce
 (PW FORM PAT-1449)
 Patent and Trademark Office

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10872 U.S. PTO
09/993967



INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Applicant: YAMADA et al.

Appln. No.: Not Yet Assigned

Filing Date: Herewith

Date: November 27, 2001

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	AR					
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FOREIGN PATENT DOCUMENTS

	Document Number	Date MM/YYYY	Country	Inventor Name	English Abstract		Translation Readily Available	
					Enclosed	No	Enclose	No
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	SR							
	TR							
	UR							
	VR							

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ML	WR	U. Gruening, et al., IEDM Technical Digest, "A Novel Trench DRAM Cell with a VERTICAL Access Transistor and BuriEd STrap (VERI BEST) for 4Gb/16Gb", 1999, pp. 25-28				
ML	XR	C. J. Radens, et al., IEDM Technical Digest, "An Orthogonal 6F2 Trench-Sidewall Vertical Device Cell for 4Gb/16Gb DRAM", 2000, pp. 349-352				
	YR					
	ZR					
	AAR					

Examiner

Date Considered: 11/24/04

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